REMARKS

This amendment is filed in response to the Office Action mailed on June, 5th 2003. Applicant respectfully traverses all objections and rejections.

Claims 1, 5, and 9 have been amended to better claim the invention.

Claims 4, 8, and 12 have been cancelled as they are now incorporated into their respective independent claims.

Claim Rejections under 35 U.S.C. §112, First Paragraph

At paragraph 2.1 of the Office Action claims 1-17 were rejected under 35 U.S.C. 112, first paragraph as failing to contain an enabling description of the invention.

At paragraph 2.2 the Examiner asserts claims 1-4, 9-13 and 16 are non-enabling stating the specification lacks enablement for generating an approximate mathematical model of a portion of a system based upon hierarchical analysis.

At paragraph 2.3 the Examiner asserts claims 5-8, 14-15, and 17 are non-enabling stating the specification lacks enablement for hierarchical analysis mathematical functions.

Applicant has amended the claims 1, 5, and 9 to read "approximate mathematical model of the timing operation" in response to Examiner's assertion that the claims could cover any mathematical model. Applicant believes the change will help make the meaning and scope of the claims more clear.

Applicant respectfully urges that the specification's description, in light of the great body of prior work concerning hierarchical analysis, should be sufficiently enabling to one skilled in the art.

Page 4, lines 15-20 of the specification describes generally the prior art:

> "In *HA*, rather than basing the simulation of the design's timing operation upon the design's actual physical characteristics, the simulation instead is based upon *approximate mathematical models* of operation of portions of the design. That is, respective *mathematical models* are generated for respective functional blocks comprising the design which may be used to estimate the *timing operation* of the design. The design's timing operation is then simulated using these *approximate models*" (emphasis added)

Page 12, lines 6-16 of the specification describe the use of the prior art approximate mathematical models in the present invention:

> "More specifically, function 82 essentially is an *approximate mathematical model of the overall timing operation* of the module 65 that is based upon, but is not itself, an accurate description of the physical characteristics of the circuits, networks, etc. comprised in module 65 or blocks 60, 62, 64, and 66 comprised in module 65. Similarly, function 84 essentially is an *approximate mathematical model of the overall timing operation* of the connection 70 that is based upon, but is not itself, an accurate description of the physical characteristics of the connection 70. Also similarly, function 86 essentially is an *approximate mathematical model of the overall timing operation* of the module 67" (emphasis added)

These descriptions must be read in light of the well know body of work on hierarchical analysis. For example, Kukimoto et al. "Hierarchical Function Timing Analysis", Proceedings of 35th ACM/IEEE Design Automation Conference, June 1998 (hereinafter Kukimoto) describes in detail how to perform hierarchical analysis of a circuit using mathematical models and functions. At col. 4, 2nd paragraph, Kukimoto states:

> "Hierarchical timing analysis is performed in two steps. The first step constructs the delay model of each leaf module by a direct application of the required time algorithm described in Section 2. Arrival times at subcircuit boundaries are then determined in a topographical order from primary inputs to primary outputs using the delay models."

The subsequent paragraphs of Kukimoto go into great detail of the the models and functions used. Further, a concrete example of hierarchical timing analysis for a 2-bit adder is given in Kukimoto at col. 5, last line to col. 8, first line.

One skilled in the art would be familiar with hierarchical analysis methods such as the ones described in Kukimoto. When a skilled artisan reads that the instant invention employs a hierarchical analysis "approximate mathematical model" and "hierarchical analysis mathematical functions" he would know how to program and implement them.

Therefore, Applicant respectfully urges that specification is sufficiently enabling in its reference to the well-known hierarchical analysis method and satisfies the requirements of §112, first paragraph.

At paragraph 2.5 the Examiner asserts claims 1-17 are non-enabling stating the specification does not describe how to program the claimed invention or how to interconnect the computer components. Applicant respectfully disagrees.

MPEP Section 2106.02 at page 2100-26 column 1, paragraph 2 directs that "in some instances, it has been found that particular kinds of block diagram disclosure were sufficiently enabling to meet the disclosure requirements of 35 U.S.C. 112, first paragraph." The section goes on to state that a major factor to look for is reliance on prior art systems. Applicant contends that due to the well-known nature of hierarchical analysis, and its extensive description in prior art references like Kukimoto, the instant application is one such instance where block diagrams are sufficient.

Further Applicant asserts the specification does describe how to interconnect the computer components used in the present invention. Page 8, line 21 to page 9, line 16 teach:

> "By way of illustration, the circuitry of module 65 may be comprised in one of the processor complexes of a parallel processor of the type described in the aforesaid copending applications, and the circuitry of the other module 67 may be comprised in another processor complex of the parallel processor. The circuitry of the two modules 65, 67 may be connected together via an intercomplex network connection 70 that permits

> data from the one of the processor complexes 65 to be provided to the other processor complex 67.
>
> One or more of the function blocks (i.e., function blocks A, B) 60, 62 of module 65 may comprise sequential logic circuits that may receive inputs 50, 80 from sources (not shown) external to the design 100 and externally-generated clock signals CLK. The blocks 60, 62 may generate and supply outputs based upon the inputs 50, 80 and clock signals CLK to down-stream function block (i.e., function block X) 64 of the module 65.
>
> . . .
>
> Function block 74 may comprise sequential logic circuitry that processes the signals it receives from the block 72 based upon external signals CLK to produce outputs that are supplied to another sequential logic circuitry block (i.e., function block D) 76"

The quoted lines, as well as other portions of the specification, provide an adequate description of how to interconnect the computer components used in the present invention.

Accordingly, Applicant respectfully urges that specification is sufficient to satisfy the requirements of §112, first paragraph.

Claim Rejections under 35 U.S.C. §112, Second Paragraph

At paragraph 3.1 of the Office Action claims 1-17 were rejected under 35 U.S.C. 112, second paragraph as being indefinite for failing to point out and distinctly claim the subject matter of the invention.

At paragraph 3.2 the Examiner asserts the term "approximate mathematical model" based upon hierarchical analysis is indefinite, as used in claims 1, 9, 13, 15, and 16-17. Examiner further asserts the term "hierarchical analysis mathematical functions" is indefinite, as used in claims 5 and 14.

Applicant has amended claims 1, 5, and 9 to read "approximate mathematical model <u>of the timing operation</u>" to clarify the type of model being used. Applicant asserts

that both the term "approximate mathematical model" based upon hierarchical analysis and "hierarchical analysis mathematical functions" are adequately described in the specification.

As previously stated, the specification describes hierarchical analysis mathematical models at page 4, lines 15-20 and at 12, lines 6-16. Further, the specification describes the use of hierarchical analysis functions at page 14, lines 18-20:

> "function 90 is an HA-based estimated function of the overall timing operation of the blocks 60, 62, 64 of the module 65. Function 92 is an HA-based estimated function of the overall timing operation of the blocks 74, 76 of the module 67"

The specification also teaches that the functions are "mathematical" at page 12, lines 2-6.

> "In essence, functions 82, 84, 86 are mathematical functional abstractions, based upon the physical characteristics of the proposed design 100 in the databases 46, 48, that may be used to estimate the overall timing operations of module 65, connection 70, and module 67, respectively, as a functions of the inputs 50, 80 and clock signals CLK provided thereto."

One skilled in the art would be familiar with the meaning and definition of "hierarchical analysis." As previously stated, the Kukimoto reference describes in depth the hierarchical analysis method and functions used with it. Therefore, from the description in the specification, and in light of the prior art, both terms would have definite meaning to one skilled in the art

Therefore, Applicant respectfully urges that application is sufficiently definite in its reference to the well-known hierarchical analysis method to satisfy the requirements of §112, second paragraph.

Claim Rejections under 35 U.S.C. §102

At paragraph 4.1 of the Office Action claims 1-12 and 16 were rejected under 35 U.S.C. 102(b) as being anticipated by Shepard et. al, "Design Methodology for the S/390 Parallel Enterprise Server G4 Microprocessors", IBM Journal of Research and Development, Vol 41 No. 4/5, pp. 515-547 (July 1997) (hereinafter Shepard).

As set out in representative claim 1, the present invention comprises in part:

> 1. A computerized method for use in simulating an operation of an electronic system, said method being carried out using a computer system, said method comprising the steps of:
>
> ***generating a physically-accurate description of the timing of a first portion of said system, said physically-accurate description comprising actual physical characteristics of said first portion;***
>
> generating an approximate mathematical model of the timing of a remaining portion of said system, said model being based upon hierarchical analysis of said remaining portion; and
>
> using both said physically-accurate description and said approximate model to simulate the timing operation of said system.

Shepard discloses a design methodology for use with the G4 microprocessor. While many aspects of design and verification are covered in Shepard, the timing analysis methods are discussed from pages 527 to 531. Shepard states, "as with all key analysis processes on the G4 design, a hierarchical approach is used" in the timing analysis (page 528, first paragraph). In particular, two levels of hierarchy are employed. In the first level, the transistor diagrams are abstracted into "macros," that take the form of either "black" or "gray" box abstractions (page 528, first paragraph and page 529, last paragraph to page 530). In the second level, global interconnect models are used to combine the "black" and "gray" boxes. (page 528, first paragraph and page 530, first paragraph to page 531). The hierarchical analysis yields an overall timing result.

Applicant respectfully urges that Shepard does not disclose the present inventions "***generating a physically-accurate description of the timing of a first portion of said system, said physically-accurate description comprising actual physical characteristics of said first portion***" and "***using both said physically-accurate description and said approximate model to simulate the timing operation of said system.***" The present invention employs both a physically-accurate description of a portion of a system and hierarchical analysis of another portion of the system to achieve greater accuracy than what hierarchical analysis could achieve alone. Shepard merely performs hierarchical analysis on the entire system. Therefore, Shepard is an example of the type of prior art system, such as the one shown in Fig. 6 of the specification, which the instant invention improves upon.

Accordingly, Applicant respectfully urges that Shepard is legally precluded from anticipating the presently claimed invention under 35 U.S.C. §102 because of the absence of Applicant's ***physically accurate description of the timing of a first portion of said system*** and the absence of Applicant's ***using both said physically-accurate description and said approximate model to simulate the timing operation of said system.***

Claim Rejections under 35 U.S.C. §103

At paragraph 5.1 of the Office Action claims 13-15 and 17 were rejected under 35 U.S.C. 103(a) as being anticipated by Shepard et. al, in view of Luk et. al, "Visualizing Reconfigurable Libraries for FPGA's" IEEE Conference Record of the Thirty-First Asilomar Conference on Signals, Systems & Computers, Vol. 1, pp. 389-393 (Nov. 1997) (hereinafter Luk).

As Examiner explains, Luk merely describes the desirability of circuit simulation using a visualization system including a user interface that provides views of design structure and behavior (page 390, col. 1). Luk makes absolutely no mention of "***gener-***

ating a physically-accurate description of the timing of a first portion of said system, said physically-accurate description comprising actual physical characteristics of said first portion" and "***using both said physically-accurate description and said approximate model to simulate the timing operation of said system.***" Therefore, Applicant respectfully urges the combination of Shepard and Luk does not render the claimed invention obvious under 35 U.S.C. §103.

Applicant believes this application is now in condition for allowance and early favorable action is respectfully requested.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,

James A. Blanchette
Reg. No. 51,477
CESARI AND MCKENNA, LLP
88 Black Falcon Avenue
Boston, MA 02210-2414
(617) 951-2500